-compensation means for reducing an offset level induced in the processed analog signal by the analog signal processing means, and comprising:

-first means connected to the system for temporarily fixing a level of the analog signal at the system input and at the second input; and

-second means connected to the ADC output for storing the output signal associated with the fixed level; and

-third means connected to the second means and to the signal processing path for affecting the signal processing after releasing the level, under control of the stored output signal.

8.(Once Amended) An electronic circuit with analog-to-digital converter means with a cascaded configuration, wherein the configuration comprises:

-a configuration input for receiving an analog input signal;

-a configuration output for providing a digital output signal;

-first stage connected to the configuration input and comprising:

-a first ADC converter, being of the flash-type and having a ladder of resistors, and having a digital

output for providing a digital output signal and an analog output for providing an analog output signal;

-an array of multiple switches, each respective one thereof coupled between a respective node in a respective pair of interconnected ones of the resistors and the analog output;

-a register connected to the digital output; and

-control logic connected between the register and the array for selectively controlling the switches depending on the output signal stored in the register;

-a second stage having:

-a first analog input connected to the configuration input;

-a second analog input connected to the analog output;

-a [combining] subtracting circuit [connected to] for subtracting the [first and] second analog input[s for providing] from the first analog input to provide, at a circuit output, a [combination of] difference analog signal[s received at the first and second analog inputs];

-a second ADC having an ADC input connected to the circuit output.

9.(Once Amended) An electronic circuit having a circuit input and a circuit output comprising:

-a subtracting circuit having a first input, a second input, and a difference output being the difference between said first and second inputs, said first input being connected to said circuit input;

-an ADC with a flash analog-to-digital converter (FADC) having a ladder of resistors and being connected to said difference output;

-an array of multiple switches, each respective one thereof coupled between a respective node in a respective pair of interconnected ones of the resistors and an output node, said output node being connected to said second input; and

-control logic connected to the array for selectively controlling the switches.

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11. (Once Amended) The circuit of claim 9, wherein:

-the circuit comprises a further array of multiple further switches, each respective one thereof coupled between the respective node in the respective pair of interconnected ones of the resistors and a further output node; said further output node being connected to a third input of said subtracting circuit.

12. (Once Amended) A method of signal processing, the method comprising:

-receiving an analog input signal at a[n] first input;

-receiving an analog correction signal at a second input;

-processing [the] a corrected analog input signal resulting from a combination of said analog input signal and said analog correction signal;

-converting the [processed] corrected analog input signal into a digital output signal, the method further comprising:

-temporality fixing a level of the analog input signal at the first input and of the analog correction signal at the second input;

-storing the digital output signal associated with the fixed level;

-releasing the level; and

-affecting the signal processing under control of the stored output signal after releasing the level.

13.(Once Amended) The method of claim 12, wherein the affecting comprises:

-creating [an] the analog correction signal at the second input on the basis of the stored digital output signal; and

-modifying the processing of the analog input signal at the first input under control of the analog correction signal at the second input.

REMARKS

Claims 1-15 are pending in the present application. Reconsideration of the present application, as amended, is respectfully requested.

In the Office Action, the Examiner objected to FIGs 1-3, 11 and 13. In response, FIGs 1-3, 6 and 11-13 have been amended to overcome the Examiner's objections and correct other informalities. Further, the specification has been amended for conformance with the amended figures. Proposed corrected FIGs 1-3, 6 and 11-13 are enclosed. Applicant respectfully requests withdrawal of the drawings objection and approval of the enclosed proposed drawing corrections.

Claims 1-4, 7 and 9-15 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,282,515 (Patterson) in view of U.S. Patent No. 5,436,629 (Mangelsdorf). Claims 5-6 and 8 were rejected under 35 U.S.C. §103(a) as being unpatentable over the references as applied to Claims 1-4, 7 and 9-15 and further in view of U.S. Patent No. 3,906,488 (Suarez). In response, Claims 1, 8, 9 and 11-13 have been amended and Claim 10 has been canceled without prejudice. It is respectfully submitted

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